

Edited by Bill Travis and Anne Watson Swager

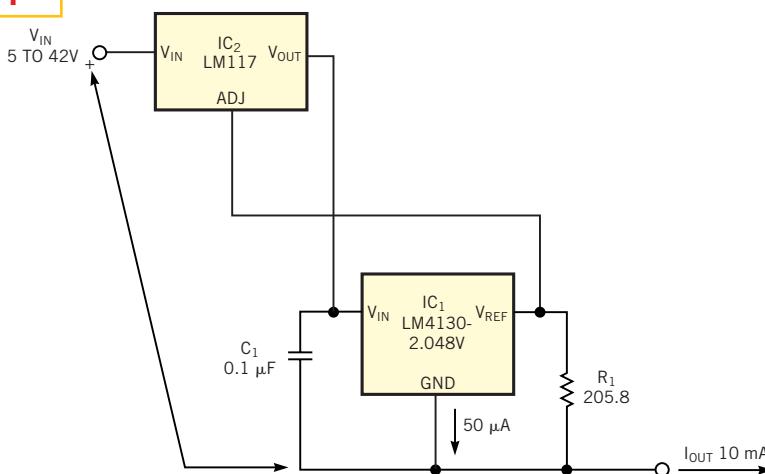
Current source has high output impedance

Clayton B Grantham, National Semiconductor, Tucson, AZ

A REFERENCE CURRENT SOURCE needs high accuracy, low temperature drift, and high output impedance. Available IC current sources come with some of these features. However, at current levels greater than 1 mA, their output impedance decreases to less than 10 M Ω . **Figure 1** shows a composite 10-mA current-source configuration that has a compliance voltage of 5 to 42V, a set-current error of less than 1%, a temperature drift of less than 45 ppm/ $^{\circ}$ C, and an output impedance of greater than 100 M Ω . One application of this accurate 10-mA current source with high impedance is as a 4- to 20-mA current-loop calibration reference that has a maximum loop voltage of 40V and that operates over the -40 to $+85^{\circ}$ C industrial-temperature range.

IC₁'s V_{REF} output and R₁ set I_{OUT}. I_{OUT} equals V_{REF}/R₁ plus IC₁'s bias current, which is typically 50 μ A. This bias current is a small error of less than 0.05% at I_{OUT} = 10 mA and changes by only 10 μ A over -40 to $+85^{\circ}$ C. Changes in V_{REF} and

Figure 1



This composite configuration of a voltage reference and a voltage regulator has high output impedance.

R₁ over temperature more directly contribute to I_{OUT}'s accuracy and temperature coefficient. Inexpensive resistors with 0.1% tolerances and 25 ppm/ $^{\circ}$ C drift over temperature are common. The LM4130 has a V_{REF} grade of 0.05% and 20 ppm/ $^{\circ}$ C over -40 to $+85^{\circ}$ C. Thus, the worst-case current-setpoint error is within 0.15% and 45 ppm/ $^{\circ}$ C, which results in an upper limit on the current error over temperature of 0.45%, or 45 μ A.

The circuit's high performance would degrade if its output impedance were not very high. The circuit's output impedance is an undesirable parasitic in parallel with I_{OUT}. The product of IC₁'s line regulation times IC₂'s line regulation determines the current source's output impedance. IC₂'s 1.2V output sets IC₁'s input-minus-output to a near constant. IC₁'s V_{REF} over R₁ sets I_{OUT}, which is twice

removed from V_{IN}, V_{REF} of IC₁ has an overtemperature line regulation of 500 ppm/V, and IC₂'s output has an overtemperature line regulation of 350 ppm/V. Output impedance is greater than 300 M Ω , which is good, if you calculate it using only the line-regulation effects. Although line regulation is the dominant source of output impedance, other thermal errors beyond line regulation degrade the potential of keeping very high output impedance over temperature. Bench measurements made on the composite showed output impedance greater than 300 M Ω at 25 $^{\circ}$ C and 100 M Ω over -40 to $+85^{\circ}$ C. (DI #2544)

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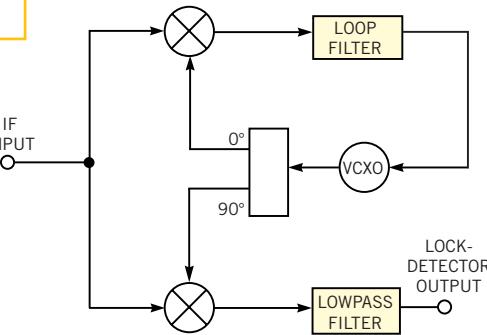
Novel method detects lock in Costas loops

MR Raghavendra, ISRO Satellite Centre, Bangalore, India

IN THE WELL-ESTABLISHED lock-detection scheme for conventional PLLs, the VCO or VCXO local oscillator splits the output into 0 and 90° signals (Figure 1). The incoming IF signal mixes with the 0 and 90° signals to perform phase locking and lock detection, respectively. This method gives unambiguous results even under noisy conditions.

For Costas-loop systems for binary-phase-shift-keying demodulation, the demodulation process uses both the 0 and the 90° signals. Thus, these signals are unusable for lock detection.

Instead, simple Costas-loop systems generally use level detection as the lock-detection method (Figure 2a). This straightforward method involves detect-



A conventional PLL uses 0 and 90° signals for phase locking and lock detection.

level equals 0. In the unlocked condition, the two data levels are equal. The scheme detects this difference to indicate lock. Unfortunately, this method can give ambiguous results under noisy conditions.

You can adopt a similar method in modified Costas loops for QPSK (quadrature-phase-shift-keying) demodulation (Figure 2b). In the unlocked condition, a beat-frequency component is

present along with the data. In the lock condition, this beat-frequency component disappears. Hence, the detected I and Q data levels are higher in the un-

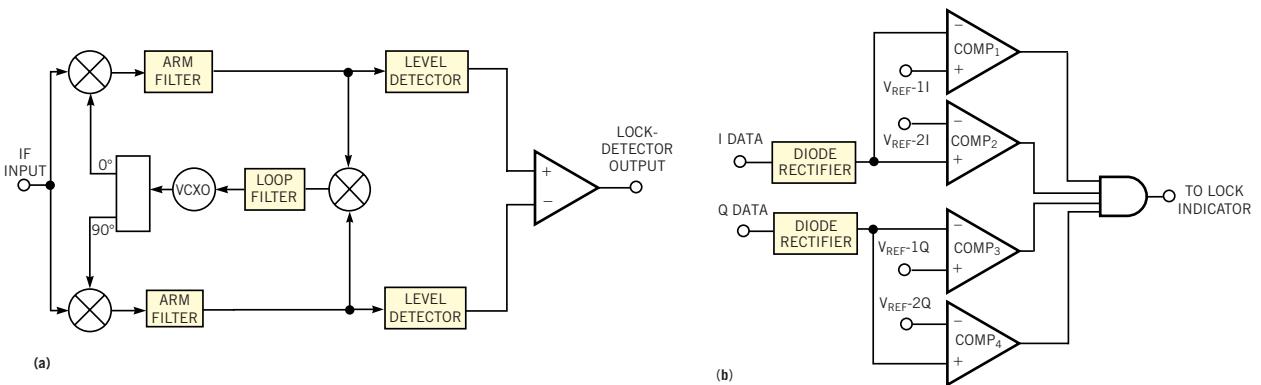
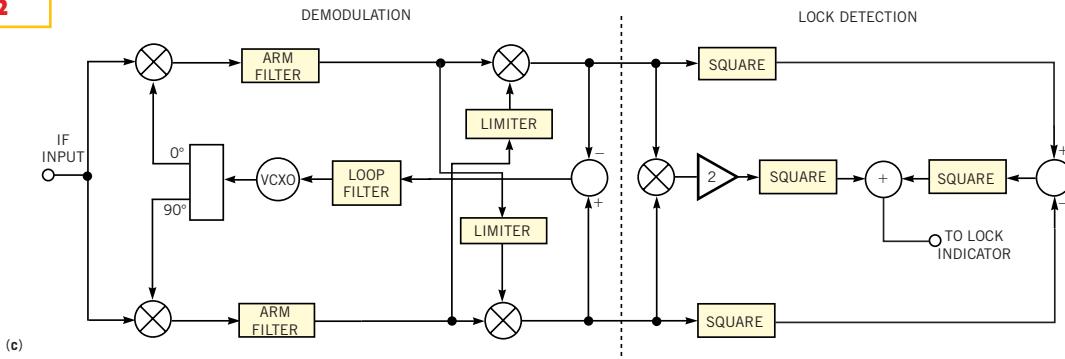


Figure 2



Various lock-detection schemes for Costas-loop systems suffer from problems. Level-detection (a) and a similar method (b) can give ambiguous results under noisy conditions. A coherent method (c) gives unambiguous results but is complex.

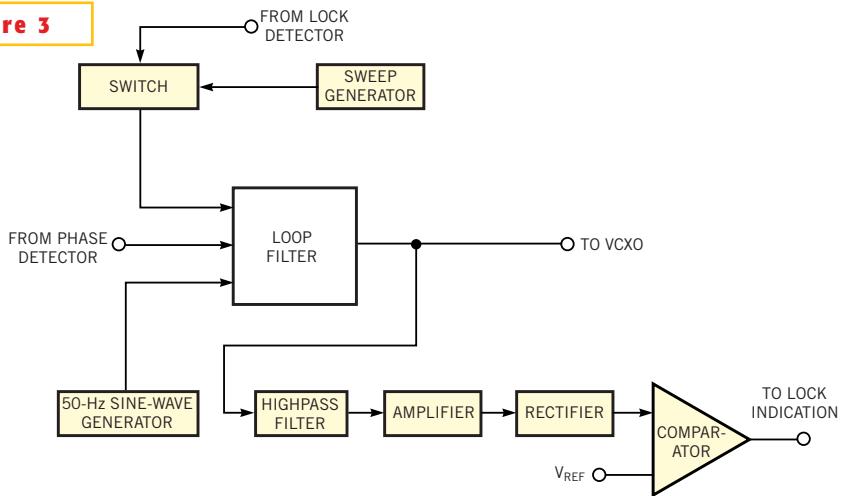
locked condition than in the locked condition. By detecting this difference in levels, you can determine the locked condition. This method is not free of ambiguities under noisy conditions because the detected levels change with levels of noise. Thus, reference-voltage settings for level comparison are critical. At some levels of noise, level comparison becomes almost impossible; under such conditions, this method of lock detection fails.

The coherent method illustrated in **Figure 2c** gives ambiguity-free lock detection for modified Costas-loop systems. Unfortunately, this method is complex, and the hardware realization is as complex as the demodulation process itself.

Figure 3 presents a new method of lock detection with much less hardware complexity. You can adopt this level of detection for any PLL system. The underlying principle of this method is that when the PLL is in lock, it tracks and neutralizes all of the low-frequency modulations within the loop. Therefore, if the system introduces a low-frequency, low-level modulation, such as at the loop-filter input, into the loop, then when the loop is locked, the low-frequency signal at the output of loop filter disappears. The presence or absence of the signal at the output of the filter provides unambiguous lock detection.

The circuit in **Figure 3** implements this method in a 375-MHz QPSK demodulator with a loop bandwidth of 10 kHz. This method involves injecting a low-level, 50-Hz sine wave at the input of

Figure 3



An improved lock-detection scheme introduces a low-frequency, low-level modulation into the loop. When the loop is in lock, this low-frequency signal at the output of the loop filter disappears.

the loop filter, which is an active filter, and injecting a sweep signal of 2 Hz, which speeds lock acquisition. If you use a passive filter in place of the active filter, you can apply the signal at the input of VCXO after the loop filter, that is at the input of the amplifier after the passive loop filter.

The scheme taps the output of the loop filter and filters out the sweep signal. The scheme then amplifies the 50-Hz signal to compensate for attenuation in the loop filter and rectifies the signal to give a dc voltage to indicate its presence. When the loop is in lock, the 50-Hz signal disappears, and the rectifier output is zero. The lock-indication output also cuts off the sweep. The 50-Hz signal re-

mains connected to the loop filter even during lock. The presence of this signal at the input of the loop filter does not degrade the demodulator performance because the level is low. You choose 50 Hz as the injected signal frequency because 50 Hz is considerably higher than the sweep-signal frequency and considerably lower than the loop bandwidth.

The performance of this method is effective even under very noisy conditions, such as when the input's E_b/N_0 (energy-per-bit-to-noise) figure is 3 dB. Previous methods give ambiguity-free results only at E_b/N_0 levels of 7 or 8 dB. (DI #2545)

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Coax connectors make low-cost test pieces

Richard M Kurzrok, RMK Consultants, Queens Village, NY

YOU CAN READILY CONSTRUCT low-cost test pieces using coaxial panel jacks without pc boards or enclosures (**Figure 1**). Some engineers and technicians occasionally use this construction technique, but the versatility of the technique is not well-known. You can design

and construct these low-cost test pieces for a variety of passive circuits using tee, pi, el, or bridged-tee networks. Other simple circuits are also amenable to this type of construction. These circuits include highpass filters, minimum-loss pads, transformers, amplitude equalizers,

and feedthrough terminations. The technique applies to all commercial, industrial, and educational breadboard units that require a quick-and-dirty implementation. The test pieces are useful for low-cost laboratory experiments on passive circuits at reasonably high frequen-

cies. The quasi-open “enclosure” for the test pieces provides good visibility of components and solder joints.

The 50Ω BNC is a popular coaxial panel connector, and significant cost differences exist between military and commercial versions. Some panel jacks come with number 3-48 tapped holes. You can drill these holes out for number 4-40 clearance. This application accommodates minor differences in panel-jack hole spacing.

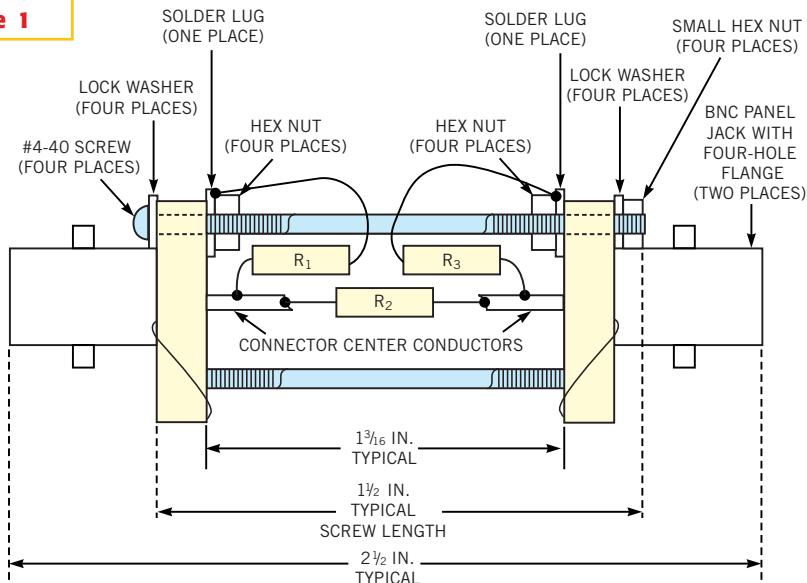
Using a single panel jack with a solder lug, you can construct a one-port circuit, such as a termination or standard mismatch. You can fabricate a two-port circuit using two panel jacks mechanically secured to each other with four 4-40 stainless-steel machine screws and ancillary hardware, such as hex nuts, lock washers, and solder lugs. The four screws provide electrical-ground continuity between the two panel jacks. You create simple passive circuits by soldering components, such as resistors, inductors, and capacitors, to the panel jacks’ center conductors and the ground lugs. You assemble three screws to the panel jacks before soldering and add the fourth screw after soldering.

The test piece in **Figure 1** is a pi-section fixed attenuator. This 6-dB, 50Ω attenuator uses 1/4W composition and carbon-film resistors with 5% tolerances. The nominal value of series resistor R_2 is 36Ω, and the shunt resistors, R_1 and R_3 , are nominally 150Ω. From 2 to 150 MHz, the measured attenuation is 6 ± 0.2 dB. At 50 MHz, the measured attenuation is 6.4 dB.

You can also create a dc block using this construction technique by placing a series capacitor between the panel-jack center conductors. The 0.1-μF CK05 capacitor has a tolerance of 10%. From 300 kHz to 30 MHz at a 50Ω impedance, the measured insertion loss is less than or equal to 0.1 dB. At 50 MHz, the measured insertion loss is 0.2 dB.

You can also achieve a pi-section low-pass filter with a 9.6-MHz cutoff frequency at a 50Ω impedance level using a

Figure 1



NOTES:
 R_1 AND R_3 SOLDERED TO ONE CONNECTOR CENTER CONDUCTOR AND ONE SOLDER LUG.
 R_2 SOLDERED TO TWO CONNECTOR CENTER CONDUCTORS.

You can easily construct a pi-circuit fixed attenuator using two BNC panel jacks, series resistor R_2 , and shunt resistors R_1 and R_3 .

TABLE 1—MEASURED TEST DATA

Frequency (MHz)	Insertion loss (dB)
2.5	Less than 0.1
4	0.1
5	0.2
6	0.35
7	0.65
8	1.25
9	2.2
9.6	3.0
10.5	4.2
12	6.7
15	11.8
20	19.5
25	25.5

series inductor and two shunt capacitors. You can characterize the filter as a single constant-K section using image parameters or as a three-pole Butterworth unit using modern network theory. Shunt input and output capacitors are 330-pF polypropylene units with 5% tolerances. A 1.66-μH series inductor comprises 18

turns of number 26 magnet wire wound on a Micro Metals T37-2 toroid. The estimate of the inductor’s unloaded Q exceeds 100. **Table 1** shows the measured test data.

When the frequency exceeds 50 MHz, alternative design techniques are more appropriate (**Reference 1**). Similar designs are achievable using other panel jacks, such as threaded-N-connector and N types. The use of nut plates can extend the technique to three- and four-port circuits. When radiation is a problem, wrapping copper-foil adhesive tape around the four machine screws provides partial shielding. (DI #2548)

REFERENCE

1. Kurzrok, RM, “Low-cost prototyping for VHF Circuits,” *Electronic Design*, Oct 18, 1999, pg 91.

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Transistor junction monitors remote temperature

Matt Smith, Analog Devices, Limerick, Ireland

THE CIRCUIT IN **Figure 1** uses a regular, general-purpose transistor as the sensing element and a thermal-diode monitor IC to measure temperature. The ADM1021 usually connects to an on-chip thermal diode on a CPU die itself, but in this application the sensor connects to a regulator low-cost discrete npn transistor, the 2N3904. The circuit ties the transistor base and collector together to form a two-wire sensor.

A technique known as ΔV_{BE} sensing forces two currents through the base-emitter junction. By measuring the differential voltage across the junction, you can accurately determine the junction temperature. This technique avoids the problems associated with thermal measurement using thermistors or thermocouples. The output from the ΔV_{BE} sensor is approximately $2.2 \text{ mV}/^\circ\text{C}$. The ADM1021 amplifies this signal and converts it to digital format.

The circuit features a simple two-wire SMBus or I²C interface, which enables simple communication with a μC or μP . This case achieves communication using three wires on a standard PC Centronics

printer port, which makes for a simple and convenient, PC-based temperature-measuring system. A further advantage of the circuit is its inherent power dissipation of $500 \mu\text{A}$. This low level enables the circuit to obtain all its power directly from the Centronics port. A graphical-user-interface software application reads the data over the Centronics port and displays the temperature in a strip-chart format or logs readings to an Excel spreadsheet. This application is useful for environmental temperature recording.

Four unused lines on the parallel port power the circuit. Diodes provide isolation to prevent bus contention if any of the lines inadvertently drive low. A 74HC05 buffers the data and clock lines. The clock line is unidirectional, and the data line is bidirectional.

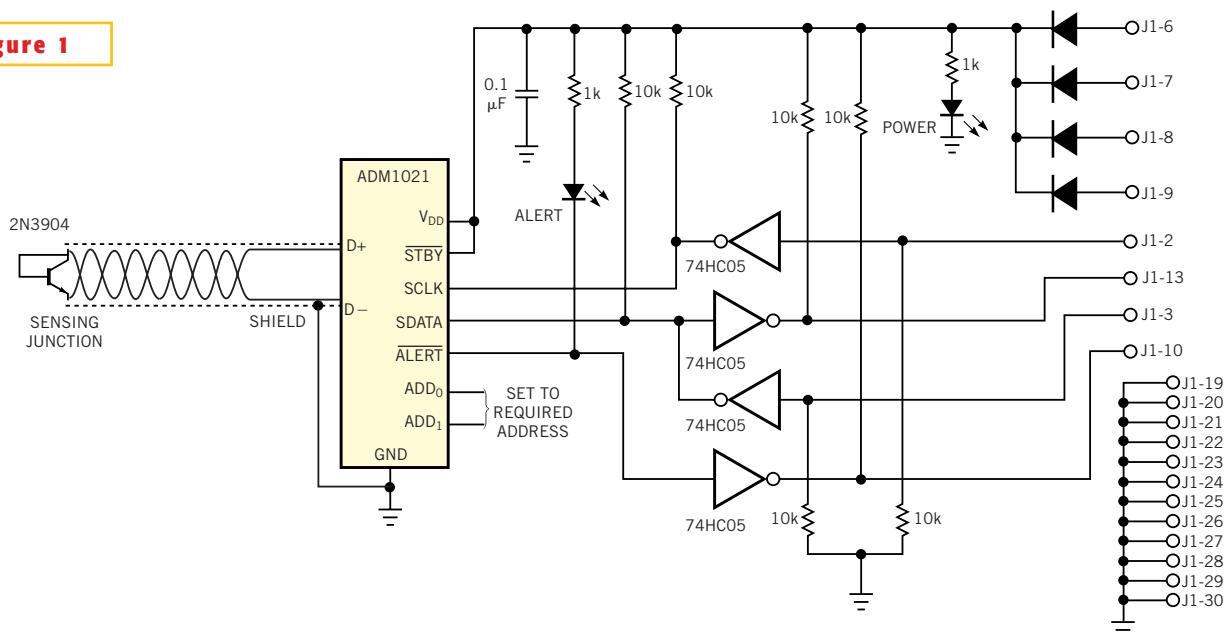
The thermal-diode monitor contains all the necessary circuitry to force differential currents through the sensing transistor. It also contains the amplifiers, scaling circuitry, and a precision ADC to convert the small differential voltages into temperature data. The remote-sensing transistor connects via a shielded

twisted pair. The shielded twisted pair is necessary only in electrically noisy environments. The circuit can accommodate temperatures of -128 to $+128^\circ\text{C}$, but in practice the usable range is more limited. The ADM1021 also contains both high- and low-limit registers and has an alert, or alarm, output. If the circuit senses a temperature that exceeds a programmed temperature limit, the IC activates the alarm output, which can drive a buzzer or warning beacon via a buffer.

Analog Devices (www.analog.com) manufactures the ADM1021 and provides PC software for Win95 or Win98 that you can use to monitor and graphically plot the recorded temperature in real time in a moving-strip-chart format. The ADM1021 also monitors its own local temperature as well as the remote-transistor temperature. You can also record temperatures and store them in an Excel format for later analysis. The recording frequency is programmable from a maximum rate of eight recordings per second. (DI #2547)

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Figure 1



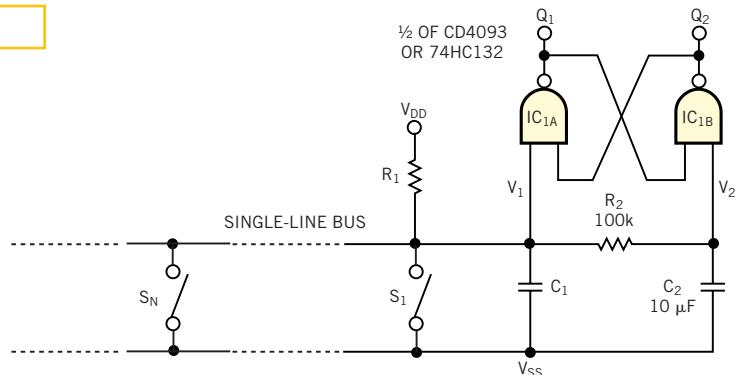
Using a regular, general-purpose transistor and a thermal-diode-sensor IC, you can monitor remote temperature and display it on your PC.

Multiple remote points control on/off switch

Tom Hornak, Portola Valley, CA

SOMETIMES, YOU NEED to remotely turn on or off a two-state system, such as a light, from multiple points. You could connect simple pushbutton switches in parallel to a single-line bus. However, if the bus simply controls a toggle flip-flop, the system must know its current state to positively ensure the new, desired state. For example, if you want to make sure the light is on, you must have visual or electrical feedback via a second line before deciding whether to toggle the flip-flop. Also, bounce-free pushbutton switches are necessary.

Figure 1

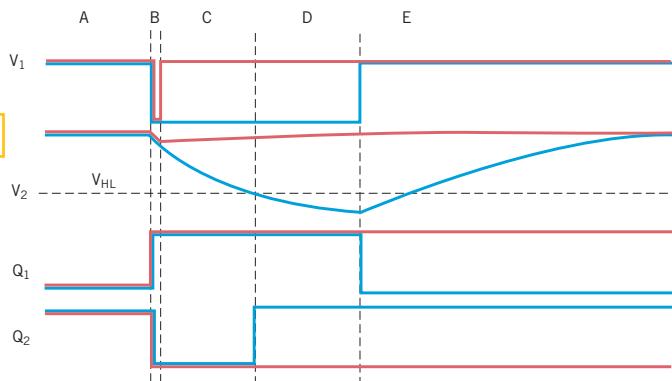


NOTE: THE VALUES OF R_1 AND C_1 DEPEND ON THE BUS CHARACTERISTICS.

A short activation of any one of the pushbutton switches, S_1 to S_N , locks the output state to Q_1 high and Q_2 low. A long activation sets the circuit to the opposite state: Q_1 low and Q_2 high.

The circuit in **Figure 1** achieves positive state control according to the length of time you activate any pushbutton switch from S_1 to S_N . An activation of a few milliseconds, for example, guarantees that the system is set to one state. An activation of 1 sec, for example, guarantees that the system is set to the other state. No visual or electronic feedback is necessary.

Figure 2



The red line corresponds to a short-activation time in section B; the blue line corresponds to a long activation time.

The circuit is a NAND R/S latch comprising two simple CMOS Schmitt trigger NAND gates. You can use half of a CD4093 or a 74HC132. **Figure 2** depicts the signal on the circuit's individual nodes. The red lines correspond to a pushbutton's "short" activation; the blue lines correspond to a "long" activation.

In **Figure 2**, in time section A, all pushbutton switches are off, both V_1 and V_2 are high, and the Q_1 and Q_2 outputs are holding the last entered state. The figure shows this arbitrarily as Q_1 low and Q_2 high, but the reverse state could also be true. When one of the switches closes (section B), V_1 goes low, but the delaying action of R_2 and C_2 keeps V_2 high. This action turns Q_1 high and Q_2 low, regardless of the previous state in section A.

If you push the button for a short time (red line in section C), V_1 returns high before V_2 can approach gate IC_{1B} 's high-to-low hysteresis threshold, V_{HL} . The circuit remains locked with Q_1 high and Q_2 low (red lines in sections C to E). If you push the button for a long time, V_1 stays low keeping Q_1 high (blue lines in sections C

and D). C_2 gradually discharges through R_2 (section C) until V_2 crosses IC_{1B} 's low-hysteresis threshold, V_{HL} , at the end of section C. As a result, Q_2 goes high. While the pushbutton is still depressed (section D), C_2 discharges even more, keeping Q_2 high. When you release the pushbutton (section E), V_1 returns high. Now, because Q_2 is also high, Q_1 goes low. C_2 charges up again via R_2 , preparing the circuit for the next activation.

Thus, a short pushbutton activation locks Q_1 high and locks Q_2 low. A long activation locks Q_1 low and Q_2 high but only after you release the pushbutton. It is important that contact bounce or reflections

from the nonterminated bus line do not influence Q_1 and Q_2 's final state.

Because the flip-flop's loop delay is negligible, the time required to completely discharge C_1 and the bus line's stray capacitance via the bus line's series resistance determine the minimum pushbutton-activation time. This time never exceeds 1 msec. The maximum short-activation time is the time over which C_2 discharges to 90% of V_{DD} , which still keeps V_2 safely above V_{HL} . For the values of R_2 and C_2 in **Figure 1**, this time is 110 msec. The minimum long-activation time is the time necessary to discharge C_2 below V_{HL} . For a worst case of

$V_{HL} = V_{DD}/2$ and for the given values of R_2 and C_2 , this minimum time is 690 msec. There is no maximum activation time. Thus, a wide tolerance exists for both the short and the long activation times, and a large margin exists between the two.

C_1 bypasses any noise that the bus may pick up from its environment. You choose the value of R_1 to keep the bus line high in spite of leakage. R_1 also needs to recharge C_1 and the bus-line capacitance to V_{DD} within a few milliseconds after you

release the pushbutton. Thus, the values of R_1 and C_1 depend on the particulars of the bus. (DI #2549)

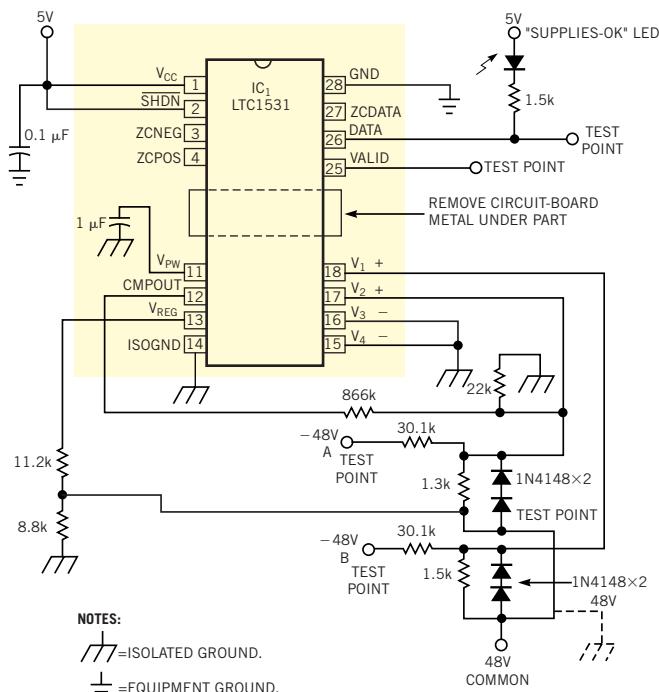
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Comparator detects failed telecomm supplies

Richard Markell, Linear Technology Corp, Milpitas, CA

YOU OFTEN NEED TO KNOW when a telecomm power supply's output drops below its nominal value. The dropout generally indicates a failure and may dictate replacement of the supply or some other form of system maintenance. The circuit in **Figure 1** uses an isolated comparator to monitor two 48V telecomm supplies (of either polarity). The comparison occurs on the 48V side of the isolation barrier. The data travels across the barrier inside the package to the output of the comparator, where a μP or another system monitor can check it. IC₁, an LTC1531 self-powered, isolated comparator, performs the isolated-comparator function. The IC has an internal capacitive barrier that provides 3000V rms of isolation between the comparator's inputs and outputs. The part provides UL-rated comparisons without an isolated supply or cumbersome optoisolators. The comparator's power and output data traverse the capacitive barrier.

Figure 1



NOTES:
 = ISOLATED GROUND.
 = EQUIPMENT GROUND.

A comparator with an isolation barrier forms the heart of a telecomm power-supply monitoring system.

The two power supplies to be monitored connect to the -48 A and -48 B points; the 48V returns connect to the "Common" input (not to isolated ground). Resistor dividers attenuate the -48V inputs; the attenuated voltages connect to the dual comparator at V_1 and V_2 . The V_{REG} pin of IC₁ provides a 2.5V regulated output, and the voltage divider consisting of the 11.2- and 8.8-k Ω resistors provides approximately 1.1V to the Common point for the 48V supplies. Connecting V_3 and V_4 to isolated ground makes the trip point a negative voltage set by the voltage divider at approximately -1.1V. The series-connected 1N4148 diodes act as crude clamps on inputs V_1

and V_2 . Clamping the inputs is necessary because the comparator function is $V_1 + V_2 > V_3 + V_4$. If the inputs were not clamped, a high voltage on one input would allow a low voltage on the other input to go undetected. The 866- and 22-k Ω resistors provide a small amount of hysteresis to stabilize the output for slow-moving inputs.

When the inequality $V_1 + V_2 < V_3 + V_4$ is false (that is, the sum of the power-supply voltages when attenuated is greater than the sum of the reference voltages), the comparator sends a signal across the isolation barrier such that the Data out-

put goes low and the LED turns on. (Note that the sense of the inequality is reversed, because you are sensing negative voltages.) The voltages in the circuit are such that when the sum of the two voltages at -48 A and -48 B are approximately -72V, the inequality is false, and the "Supplies OK" LED turns on. Thus, if one supply is "good" at -48V, the other supply is considered "bad" if it falls below approximately -24V. (DI #2541)

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